IN THE CLAIMS

1. (Previously Presented) A printed circuit board comprising:

a conductive layer;

a via transecting the conductive layer; and

an anti-pad around the via, the anti-pad comprising a pattern of conductive material having a plurality of voids,

wherein the pattern of conductive material is electrically isolated.

2. (Original) The printed circuit board of claim 1, wherein the pattern of conductive material is configured to maintain planarity of the printed circuit board.

3. (Original) The printed circuit board of claim 1, wherein the pattern of conductive material is configured to prevent settling of dielectric material in the printed circuit board near the via.

4. (Original) The printed circuit board of claim 1, wherein the via is configured for data transfer rates greater than approximately 2 GHz.

5. (Original) The printed circuit board of claim 1, wherein the pattern of conductive material is configured for data transfer rates through the via greater than approximately 2 GHz.

6. (Original) The printed circuit board of claim 1, wherein the pattern of conductive material is substantially circular in shape.

7-8. (Cancelled)

9. (Original) The printed circuit board of claim 1, wherein the conductive layer comprises a power plane.

10. (Original) The printed circuit board of claim 1, wherein the conductive layer comprises a ground plane.

11. (Original) The printed circuit board of claim 1, wherein the pattern comprises a symmetric pattern.

12. (Original) The printed circuit board of claim 1, wherein the pattern comprises an asymmetric pattern.

13. (Original) The printed circuit board of claim 1, wherein the pattern comprises a concentric circles pattern.

14. (Original) The printed circuit board of claim 1, wherein the pattern comprises a radial spokes pattern.

15. (Original) The printed circuit board of claim 1, wherein the pattern comprises an arbitrary pattern.

16. (Original) The printed circuit board of claim 1, wherein the pattern comprises a screen pattern.

17. (Previously Presented) A printed circuit board comprising:

a conductive plane;

a via signal barrel transecting the conductive plane; and

an anti-pad between the conductive plane and the via signal barrel, the anti-pad having a pattern of conductive material, wherein a signal can not be transmitted between the conductive plane and the via signal barrel, and

wherein the pattern of conductive material is electrically isolated.

18. (Original) The printed circuit board of claim 17, wherein the pattern of conductive material includes a plurality of voids.

19. (Original) The printed circuit board of claim 17, wherein the anti-pad is configured to maintain planarity of the printed circuit board.

20. (Original) The printed circuit board of claim 17, wherein the anti-pad is configured to minimize stray capacitance between the via and the conductive plane.

21. (Original) The printed circuit board of claim 17, wherein the anti-pad is configured to prevent settling of dielectric material in the printed circuit board adjacent the via signal barrel.

22. (Original) The printed circuit board of claim 17, wherein the conductive plane comprises one of a power plane and a ground plane.

23. (Original) The printed circuit board of claim 17, wherein the conductive plane comprises copper.

24. (Previously Presented) A method for forming a printed circuit board, comprising:

forming a conductive plane;

forming a via signal barrel transecting the conductive plane; and

forming a partially voided anti-pad between the conductive plane and the via signal barrel,

wherein the partially voided anti-pad is electrically isolated.

25. (Original) The method of claim 24, wherein the conductive plane comprises one of a power plane and a ground plane.

26. (Original) The method of claim 24, wherein the partially voided anti-pad is formed to maintain the planarity of the printed circuit board.

27. (Original) The method of claim 24, wherein the partially voided anti-pad is formed to minimize stray capacitance between the via and the conductive plane.

28. (Original) The method of claim 24, wherein the partially voided anti-pad is formed by removing conductive material from the conductive plane in a pattern.

29. (Original) The method of claim 28, wherein removing conductive material is performed by using an etching process.

30. (Original) The method of claim 28, wherein the pattern comprises one of a symmetric pattern and an asymmetric pattern.

31. (Original) The method of claim 28, wherein the pattern comprises a screen pattern.

32. (Original) The method of claim 28, wherein the pattern comprises one of an arbitrary pattern and a random pattern.

33. (Original) The method of claim 24, wherein the anti-pad is substantially circular in shape.

34. (Original) The method of claim 24, wherein the via signal barrel is substantially circular in shape.

35. (Previously Presented) A printed circuit board comprising:

a conductive layer;

a via transecting the conductive layer; and

an anti-pad around the via, the anti-pad comprising a pattern of conductive material having a plurality of voids, the pattern of conductive material isolated from the conductive layer,

wherein the pattern comprises an asymmetric pattern.

36. (Previously Presented) A printed circuit board comprising:

a conductive layer;

a via transecting the conductive layer; and

an anti-pad around the via, the anti-pad comprising a pattern of conductive material having a plurality of voids, the pattern of conductive material isolated from the conductive layer,

wherein the pattern comprises a concentric circles pattern.

37. (Previously Presented) A printed circuit board comprising:

a conductive layer;

a via transecting the conductive layer; and

an anti-pad around the via, the anti-pad comprising a pattern of conductive material having a plurality of voids,

wherein the pattern comprises a screen pattern.